# GOLF

*A Versatile Layout Platform*

## OVERVIEW

GOLF is a production-proven OpenAccess-based layout platform adopted by world-class semiconductor companies since 2007. GOLF features powerful layout editing functions, intuitive GUI, flexible customization and extension. GOLF provides a versatile layout editor and viewer with simplicity and flexibility. GOLF provides API in C++/TCL/PERL/PYTHON (and more on demand) to help customers develop a variety of applications. The differentiation of GOLF vs. other tools is in its capability of customization for different applications such as custom layout, analog layout automation, test structure layout automation, flat panel display layout automation, wafer-level chip-scale packaging layout automation, etc.

## HIGHLIGHTS

- Auto contact, auto slot
- Array stretch, split, chop
- Undo and redo
- Layout windows: tile/cascade, bird view
- Navigation-based forms: dock/floating
- Option forms: pop-up/minimized (prompt bar)
- Dynamic viewing: mouse zooming, command viewing
- Selection schemes: mouse select, command select
- Data creation: shapes, text, text-array, instance and array…
- Editing: stretch, align, copy, move, transform, append, cut, merge, delete, yank, paste, properties…
- Hierarchical editing: descend, push, EIP, flatten, make cell…
- Query: ruler, distance, measurement, tree, connectivity, trace…
- Verify: Calibre DRC/LVS results viewer, run Calibre DRC/LVS/RVE, IC Validator VUE Interface
- Built-in hierarchical schematic viewer
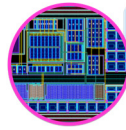
### Custom Layout
- Intuitive GUI, Advanced Functions
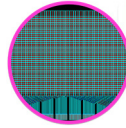- Multiple Patterning, FinFET Grid
- ECO Comparison
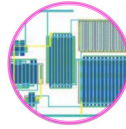
### Analog Layout Automation
- Schematic-Driven Layout
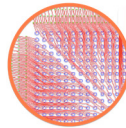- Constraint-Driven Placer
- Constraint-Driven Router

### Test Structure Layout Automation
- PCell Designer
- Test Module Generator
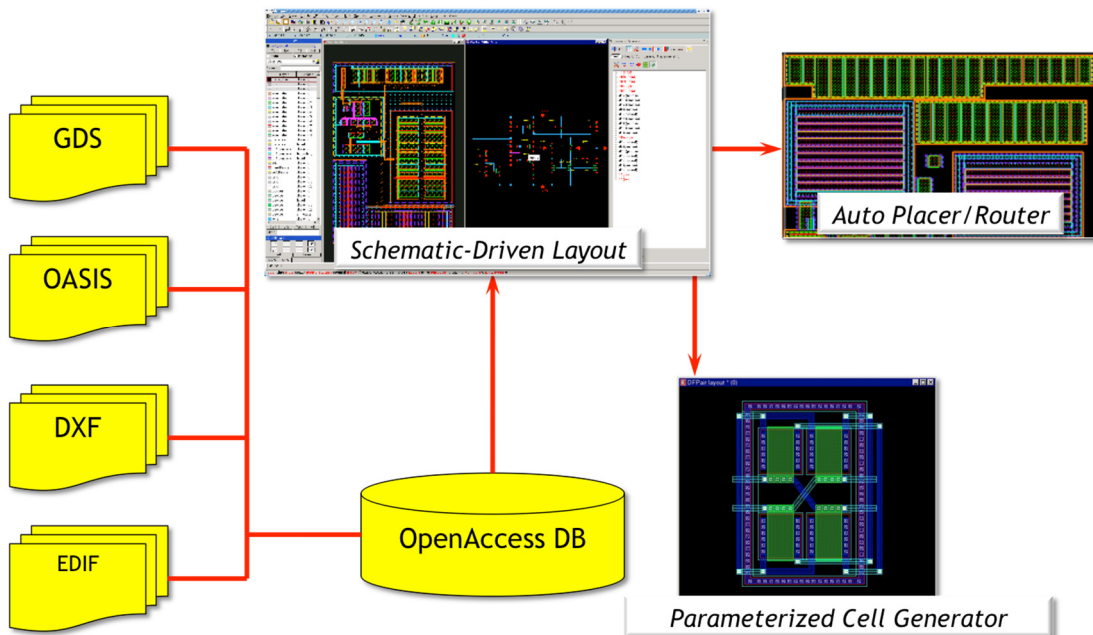- Test Structure Assembler

### Flat Panel Display Layout Automation
- Panel Designer
- Fanout Router
- WOA Router

### Wafer-Level Chip-Scale Packaging Layout Automation
- Multi-Layer/Multi-Chip RDL Router
- Dummy Insertion
- Perforate Wide Metal into Meshes



GDS

OASIS

DXF

EDIF

OpenAccess DB

*Schematic-Driven Layout*

*Auto Placer/Router*

*Parameterized Cell Generator*

## SCHEMATIC-DRIVEN LAYOUT (SDL)

SDL operates with a hierarchical connectivity model working simultaneously at all levels of the design hierarchy. This capability will alarm connectivity errors as the net is short or open. This makes designers easier to understand the complexity of interactions through the design hierarchy. SDL also supports one-to-many mapping across multiple hierarchy levels. This allows layout designers to view different layout hierarchies at the same time for efficient net tracing or debugging. The cross probing of hierarchy net tracer and Short Indicator can easily highlight the problem net. It does significantly reduce efforts and speed up the debugging processes.

- Layout realization from schematic using PCell devices
- Transistor/Resistor/Capacitor/Inductor PCell mapping
- Mapping from predefined sub-circuit layout
- Analog placer with multiple constraints: Symmetry, Proximity, Preplaced, Fixed-Boundary-Block, Boundary, Minimum Separation
- Analog router with multiple constraints: Symmetry, Topology-Matching, Length-Matching, Length-Ratio-Matching, Bounding
- Supports PCell transistors merge/split/stretch/folding functions
- Cross-probing between schematic/layout and netlist browser
- Connectivity driven editing: net propagation when creating wire, net flylines, real-time short and open detection
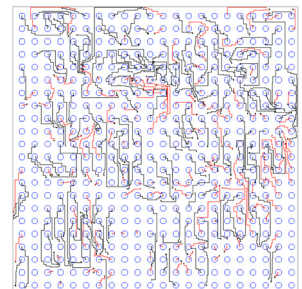- Schematic comparison in ECO flow

## PCELL DESIGNER

Evolved with the experiences and feedbacks of PCell programmers and layout engineers, GOLF provides a visualized integrated development environment (IDE) for parameterized layout design, preview, testing, debug, and documentation on layout directly. It is based on AnaGlobe's patented highly flexible and reusable hierarchical parameterized layout generator. The OpenAccess (OA) objects of the existing layout can be parameterized directly. More complicated objects such as polygon text, fingers, spiral, and runway are provided. Layout can be composed by geometric operations with object lifetime control. User-defined code (in C++/TCL/PERL/PYTHON) can still be integrated as well.
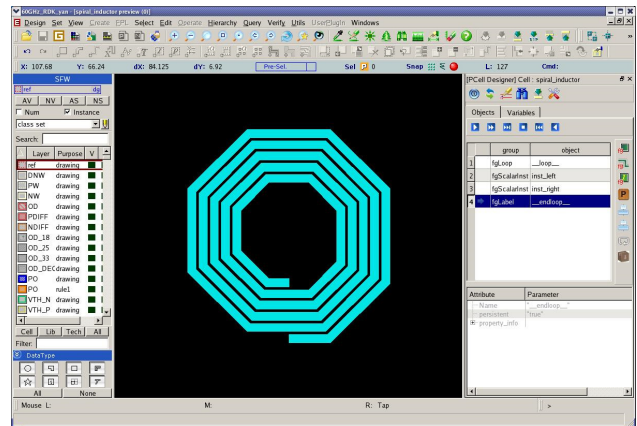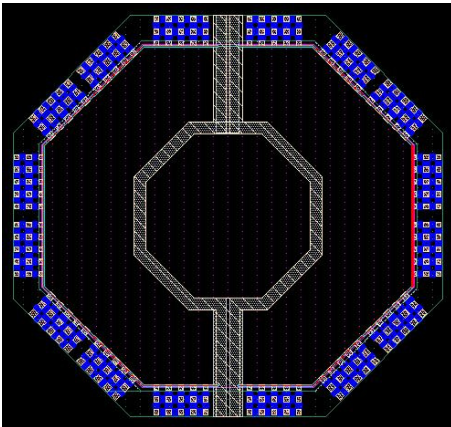


## WAFER-LEVEL CHIP-SCALE PACKAGING LAYOUT AUTOMATION

GOLF provides an integrated layout design environment that bridges the gap between the chip and package implementation.

- Multi-layer, multi-chip RDL router
- Dummy Insertion
- Perforate wide metal into meshes



AnaGlobe